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Question Paper Code : 51202

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Third Semester

Electronics and Communication Engineering

EC 1203 — ELECTRONIC CIRCUITS — I

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define an AC load line.

2. Give the advantages of self bias.

3. Consider CE amplifier with fixed bias. If $\beta = 70, R_B = 380\,k\Omega, R_C = 1.4k\Omega$, and $V_{CC} = 30\,V$, find the coordinates of Q-point.

4. How is the constant current circuit used to improve the CMRR?

5. Define gain – bandwidth product.

6. Relate rise time and bandwidth.

7. Why is non-linear distortion called harmonic distortion?

8. What is thermal resistance? Give its unit.

9. Write short notes on the desensiturity of gain.

10. Write the Nyquist criterion for stability of feed back amplifiers.

PART B — (5 × 16 = 80 marks)

11. (a) A CE transistor amplifier with voltage divider bias circuit is designed to establish the quiescent point at V_{CE} = 12 V, I_C = 2 mA and stability factor ≤ 5.1. If V_{CC} = 24 V, V_{BE} = 0.7 V, $\beta = 50$ and $R_C = 4.7k\Omega$ determine the values of resistors R_E, R_1 and R_2. (16)

Or

(b) Calculate the operating point of the self biased JFET having the supply voltage V_{DD} = 20 V, maximum value of drain current is 10 mA and gate source voltage is –3v at I_D = 4 mA. Also determine the values of R_D and R_s to obtain this bias condition. (16)

12. (a) Draw the AC equivalent circuit of a CE amplifier with voltage divider bias using hybrid parameters model and derive the equations for input impedance, output impedance, voltage gain and current gain. (16)

Or

(b) Explain an emitter coupled differential amplifier and its salient features with a neat circuit diagram. Also derive the expressions for CMRR, input impedance and output impedance. (16)

13. (a) Draw the high frequency hybrid π model for a transistor in the CE configuration and explain the significance of each component. (16)

Or

(b) Discuss the high frequency equivalent circuit of FET and hence derive gain bandwidth product for any one configuration. (16)

14. (a) Describe with neat sketch or circuit diagram the working of Class B push pull power amplifier. Prove that its maximum theoretical efficiency is 78.5%. What are its advantages? (16)

Or

(b) (i) What is cross over distortion in Class B push pull amplifier? Suggest a method to eliminate it with suitable circuit diagram. (8)

(ii) Explain the working of Class D amplifier. What is its efficiency and state its applications. (8)

15. (a) Draw a sketch and illustrate the principle of series voltage negative feed back and list the major effects of negative feed back on amplifier. (16)

Or

(b) Using illustrations, explain the effects of negative feed back on the bandwidth of an amplifier and discuss the effects of open loop gain reduction and closed loop gain. (16)

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